

IN THE CLAIMS

Please cancel claims 1-12 without prejudice.

Please amend claims 15 and 16 as follows below.

Please add new claims 17-34 that follow below.

Please accept a clean version of the entire set of pending claims as amended by this response.

CLEAN CLAIMS ARE AS FOLLOWS

1        1-12. (Cancelled)

1        13. (Unamended)        A method for assembling an

2        electronic package, comprising:

3        forming a housing which has a bond pad located on a bond  
4        shelf which has an edge;

5        forming a conductive strip along the edge of the bond  
6        shelf;

7        removing a portion of the conductive strip.

1        14. (Unamended)        The method as recited in claim 13,  
2        wherein

3        the conductive strip is formed by plating a conductive  
4        material onto the edge.

*Subc41*

15. (Amended Once) The method as recited in claim 13,  
2 wherein  
3 the portion of the conductive strip is removed by  
4 drilling a portion of the bond shelf.

16. (Amended Once) The method as recited in claim 13,  
2 further comprising:  
3 mounting an integrated circuit to the housing and  
4 connecting the integrated circuit to the bond pad.

*Subc51*

17. (New) The method as recited in claim 13, wherein  
the portion of the conductive strip is removed by  
etching away a portion of a conductive material on  
the bond shelf.

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18. (New) The method as recited in claim 13, wherein  
the conductive strip is formed along the edge of the  
bond shelf by  
masking all surfaces except for the edge of the  
bond shelf, and  
plating a conductive material onto the edge of the  
bond shelf.

1           19. (New) The method as recited in claim 18, wherein  
2           the conductive material is copper,  
3           and  
4           the conductive strip is further formed by  
5           plating gold onto the copper.

1           20. (New) The method as recited in claim 19, wherein  
2           the portion of the conductive strip is removed by  
3           drilling a portion of the bond shelf.

1           21. (New) A method of forming an integrated circuit  
2           package, comprising:  
3           providing a package housing having a first plurality of  
4           bonding pads located on a first bond shelf, the first bond  
5           shelf having a first edge;  
6           forming a first conductive strip along the first edge of  
7           the first bond shelf, the first conductive strip wrapping  
8           around the edge of the first bond shelf from at least one of  
9           the first plurality of bonding pads on the first bond shelf  
10          to a first conductor under the first bond shelf; and,  
11          removing a portion of the first conductive strip.

1           22. (New) The method as recited in claim 21, wherein

2 the first conductive strip is formed by plating a  
3 conductive material onto the first edge.

1 23. (New) The method as recited in claim 21, wherein  
2 the first conductor under the first bond shelf is a  
3 power bus.

1 24. (New) The method as recited in claim 21, wherein  
2 the first conductor under the first bond shelf is a  
3 routing trace.

1 25. (New) The method as recited in claim 21, wherein  
2 the portion of the first conductive strip is removed by  
3 drilling a portion of the first bond shelf.

1 26. (New) The method as recited in claim 25, wherein  
2 the portion drilled in the first bond shelf is a  
3 notch.

1 27. (New) The method as recited in claim 21, wherein  
2 the portion of the first conductive strip is removed by  
3 etching away a portion of the first conductive  
4 strip of the first bond shelf.

1 28. (New) The method as recited in claim 21, wherein  
2 the package housing is provided by  
3 forming a first conductive layer on a first  
4 dielectric substrate,  
5 placing a second dielectric substrate on the first  
6 conductive layer of the first dielectric substrate, the  
7 second dielectric substrate having a second conductive  
8 layer, and  
9 etching the second conductive layer to form the  
10 first plurality of bonding pads.

1 28. (New) The method as recited in claim 28, wherein  
2 the first conductive layer forms the first  
3 conductor under the first bond shelf.

1 30. (New) The method as recited in claim 28, wherein  
2 the etching of the second conductive layer to further  
3 form a second conductor, and  
4 the package housing has a second plurality of bonding  
5 pads located on a second bond shelf, the second bond shelf  
6 having a second edge, the package housing is further provided  
7 by  
8 placing a third dielectric substrate on the

9 second conductive layer of the second dielectric  
10 substrate, the third dielectric substrate having a  
11 third conductive layer, and  
12 etching the third conductive layer to form a  
13 second plurality of bonding pads,  
14 and  
15 the method further includes  
16 forming a second conductive strip along the second edge  
17 of the second bond shelf, the second conductive strip  
18 wrapping around the second edge of the second bond shelf from  
19 at least one of the second plurality of bonding pads on the  
20 second bond shelf to the second conductor under the second  
21 bond shelf.

*BS*

1 31. (New) The method as recited in claim 30, wherein  
2 the second conductive layer forms the second  
3 conductor under the second bond shelf.

1 32. (New) The method as recited in claim 30, wherein  
2 the second conductive strip is formed by plating a  
3 conductive material onto the second edge.

1 33. (New) The method as recited in claim 30, wherein  
2 the second conductor under the second bond shelf is

3 a power bus.

1 34. (New) The method as recited in claim 30, wherein  
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3 the second conductor under the second bond shelf is  
a routing trace.